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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,157	12/07/2001	Anthony J. Cachat	01AB055	6606

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EXAMINER	
HARTMAN JR, RONALD D	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,157	CACHAT ET AL.	
	Examiner	Art Unit	
	Ronald D. Hartman Jr.	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-15 and 18-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-15 and 18-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. As per claims 5 and 13, the examiner is confused by "if no localized feedback wire exists in the feedback loop", within the context of the rest of claims 5 and 13.

Is the intention of the applicant to have claims 5 and 13 claim that if no localized feedback wire exists, then determining that an unspecified feedback loops exists and then generating an error? This seems to state that if no localized feedback wire exists then you always generate an error. The examiner is confused. If the examiner understands this claim correctly, the only way to avoid an error being generated is to have a feedback wire; otherwise an error would always be generated. Is this the intent of the applicant? For examination purposes, this feature has been interpreted to mean that if there is a feedback loop lacking a feedback wire, then it is determined there exists an unspecified feedback loop in the function block diagram. Based on this determination, an error is reported to a user. Therefore, it seems that the applicant had intended to claim a feature wherein an error is reported if a localized feedback wire is missing from the function block diagram since this missing wire would dictate that there is a feedback loop that is unspecified, in other words, that is not specified correctly, and this interpretation will form the basis of any and all art rejections based on the prior art of record.

In the interest of clarity, the applicant is kindly asked to define specifically what is meant by a "localized feedback wire". How is a localized feedback wire any different than a feedback wire of a feedback loop? For examination purposes, the examiner will treat each as one and the same since the examiner cannot determine what is meant by "localized".

Also, in the interest of clarity, the applicant is kindly asked to specifically define what is meant by "unspecified feedback loop".

Since the examiner is confused as to what is intended by the claiming of "localized feedback wire" and "unspecified feedback loop", the examiners interpretations, with respect to the rational already explained above with reference to claims 5 and 13 will be applied with respect to any and all prior art rejections.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-3, 5-15 and 18-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

As per claim 1, the claim has been written in an "IF THEN" methodology, wherein IF an unspecified feedback loop exists THEN reporting an error to a user, and although this situation produces a tangible output and therefore meets the requirements under 35 U.S.C. 101, there exists another situation for which there does not appear to be a tangible result. That is, what occurs when there is not an existence of an unspecified feedback loop? That is, when the IF part of the IF THEN fails to be satisfied. Under this condition, there is currently no tangibility since there is no tangible output claimed for this condition, and therefore claim 1 does not fully encompass a tangible output for all conditions of the IF THEN statement.

This rational is applied to pending claims 13, 25 and 26, wherein claim 13 and 25 refers to an extra localized feedback wire as opposed to the unspecified feedback loop of claims 1 and 26.

It does not appear that any of the pending dependent claims alleviate this deficiency and therefore they are rejected equally under 35 U.S.C. 101.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-7, 9-10, 13-15, 18-19, 21-22, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al., U.S. Patent No. 6,931,288.

The applied reference has a common Assignee and Inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1, Lee et al. teaches a computer implemented method comprising:

- determining input data availability for the inputs of a plurality of function blocks (e.g. C7 L43-48);
- automatically assigning an execution order number (e.g. interpreted to be functionally equivalent to determining the execution order; also see rational applied to claim 7 below) to at least one of the plurality of function blocks based in part upon a determination of whether an input data source is derived from a controlled process (e.g. C1 L19-21) and whether the input data source is part of a feedback loop (e.g. C7 L43-48 and C8 L18-30); and
- determining whether an unspecified feedback loop exists in the function block diagram and reporting an error to a user if an unspecified feedback loop exists in the function block diagram (e.g. Interpreted to functionally correspond/equivalent to when a feedback loop exists that is incorrectly connected; Abstract "wiring error indications").

As per claim 2, determining a feedback loop existing in the function block diagram and assuming data availability for function blocks in the feedback loop are adequately taught by Lee et al. (e.g. C8 L14-30).

As per claim 3, determining whether a localized feedback wire is associated with a function block input in the feedback loop and assuming data availability for the function block input associated with the localized feedback wire are features believed to be inherent to Lee et al. as there does not seem to be any difference between a feedback wire or localized feedback wire.

As per claim 5, determining that an unspecified feedback loop exists if no localized feedback wire exists in the feedback loop, as best understood, is adequately contemplated by the disclosure of Lee et al. since Lee et al. teaches the determination or wiring error indications and since an unspecified feedback loop would be a loop that would be determined to be wired incorrectly (See claim 1).

As per claim 6, determining whether an extra localized feedback wire exists in the function block diagram and generating an error if an extra feedback wire exists in the function block diagram, as best understood, is adequately contemplated by the disclosure of Lee et al. since, as already mentioned, Lee et al. teaches indicating whether wiring connections are correct or incorrect (Abstract) and an extra wire would be considered to be a wire that is incorrectly connected.

As per claim 7, assigning an execution order number to each of the function blocks appears to be a feature that is functionally equivalent to determining the execution order. That is, there does not appear to be any patentable difference between assigning an execution order by using letters, numbers or any other methodology since the function being performed, that is, assigning an execution order, does not change based on what characters or notations are used, and therefore to use a number as a way of designating the execution order appears to be a feature that is functionally

equivalent to the determination of the execution order since there must be some way of keeping track of the execution order, if not, the invention would fail to operate as disclosed.

As per claim 9, assuming data availability for a first input of a first function block if the first input is associated with an input reference is adequately disclosed by Lee et al. (e.g. C8 L1 –13).

As per claim 10, the rational behind the rejection of claim 7 is applied equally herein.

As per claim 13, and as best understood in light of the comments made above, the rejection of claim 1, from above, is applied equally herein.

Also, it is noted that Lee et al. also teaches generating a control routine from the function block diagram (e.g. C7 L32-42).

As per claim 14, the rejection of claim 2, from above, is applied equally herein.

As per claim 15, the rejection of claim 3, from above, is applied equally herein.

As per claim 18, the rejection of claim 6, from above, is applied equally herein.

As per claim 19, the rejection of claim 7, from above, is applied equally herein.

As per claim 21, the rejection of claim 9, from above, is applied equally herein.

As per claim 22, the rejection of claim 10, from above, is applied equally herein.

As per claims 25-26, the rejection of claims 1, 13 and 18, from above, are equally applied herein.

Allowable Subject Matter

4. Claims 8, 11, 20 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As per claims 8, 11, 20 and 23, the prior art of record fails to teach determining data availability for the input of a first function block if an execution order number has been assigned to the second function block, in combination with the other claimed features and or limitations as claimed.

Claims 12 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As per claims 12 and 24, the prior art of record fails to teach assigning an execution order number, wherein a next available execution number is assigned to a first function block if data is available for all inputs of the first function block, in combination with the other claimed features and or limitations as claimed.

Conclusion

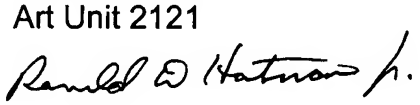
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald D. Hartman Jr. whose telephone number is (571) 272-3684. The examiner can normally be reached on Mon.-Fri., 11:00 - 8:30 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (571) 272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ronald D Hartman Jr.
Patent Examiner
Art Unit 2121



May 29, 2006
RDH